

FIG.1

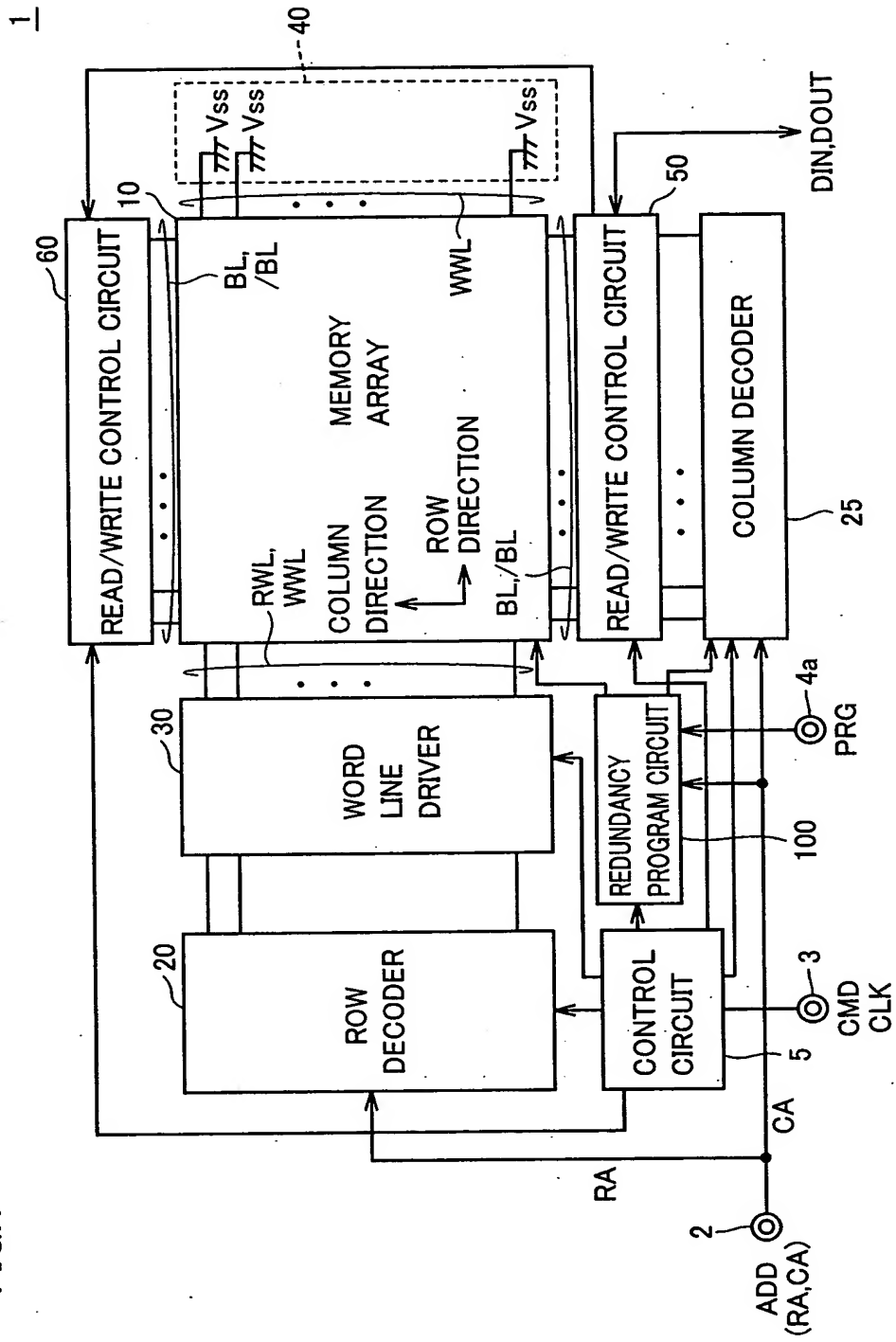


FIG.2

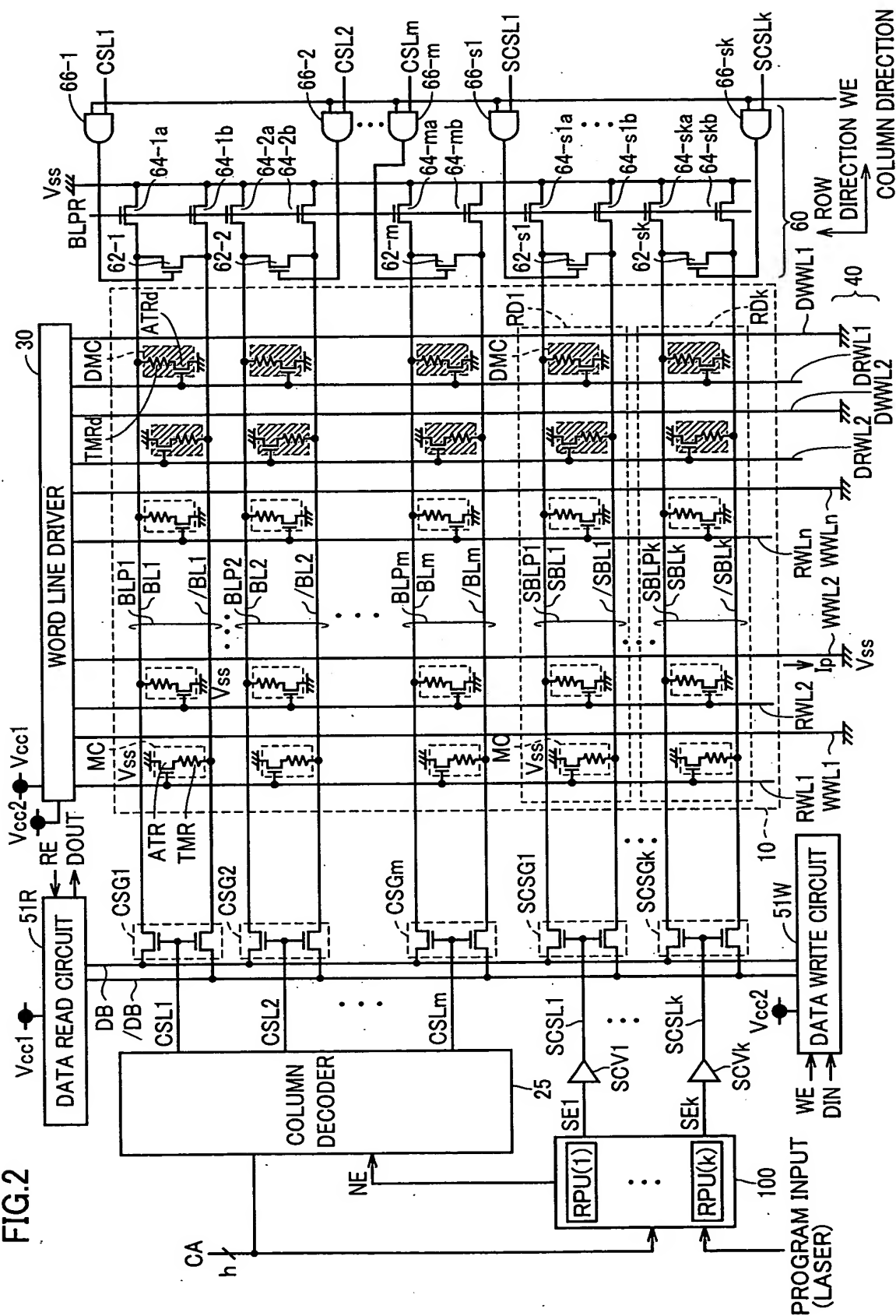


FIG.3

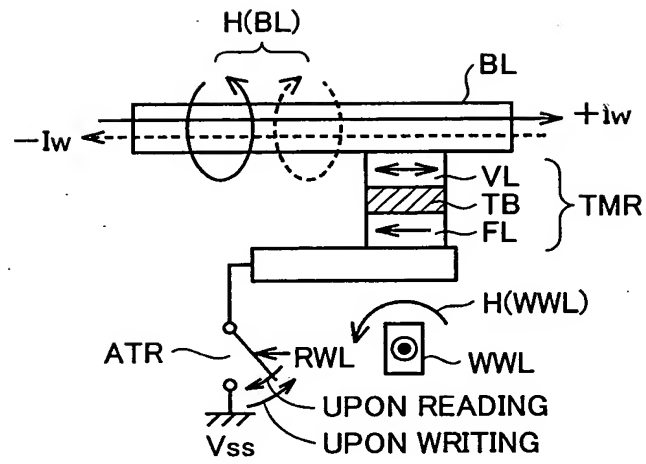


FIG.4

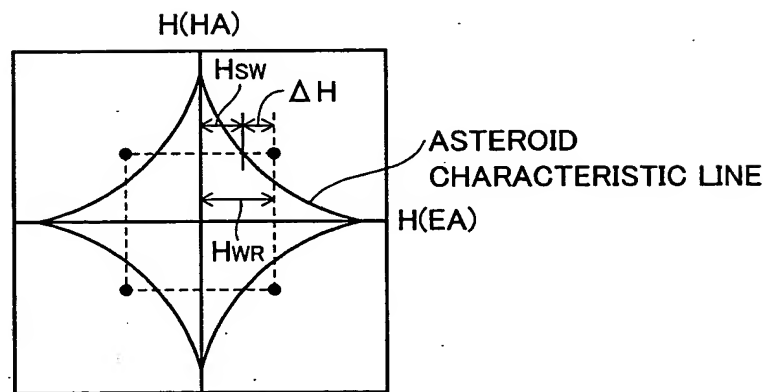


FIG.5

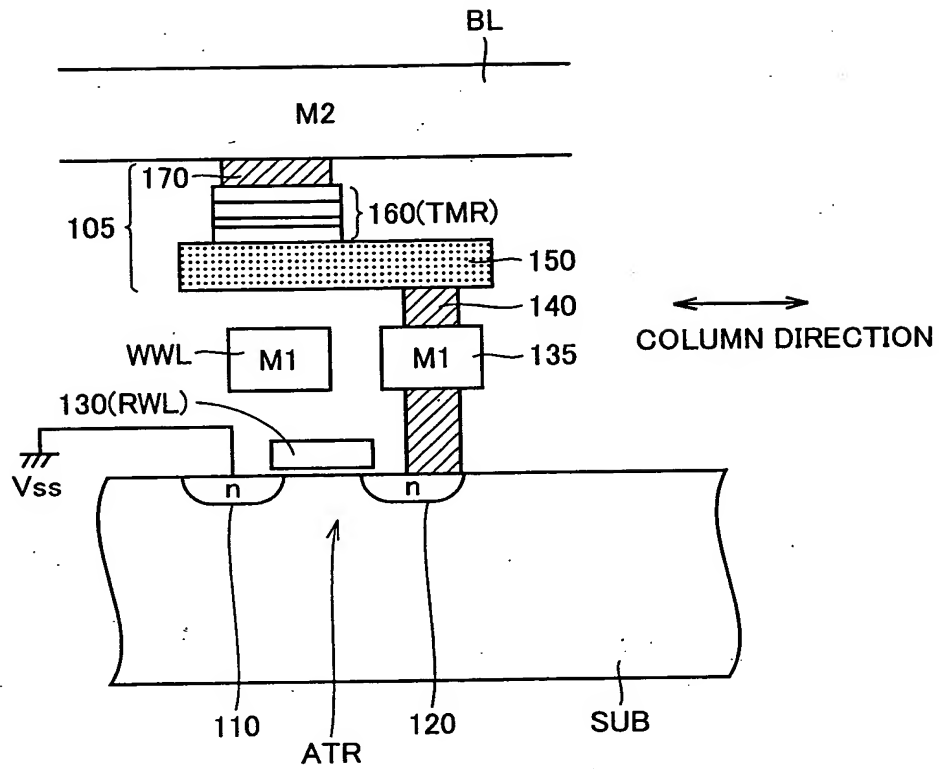


FIG.6

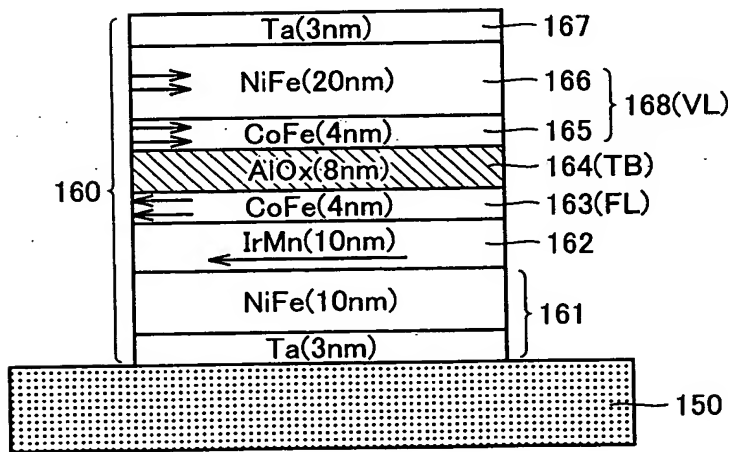


FIG.7

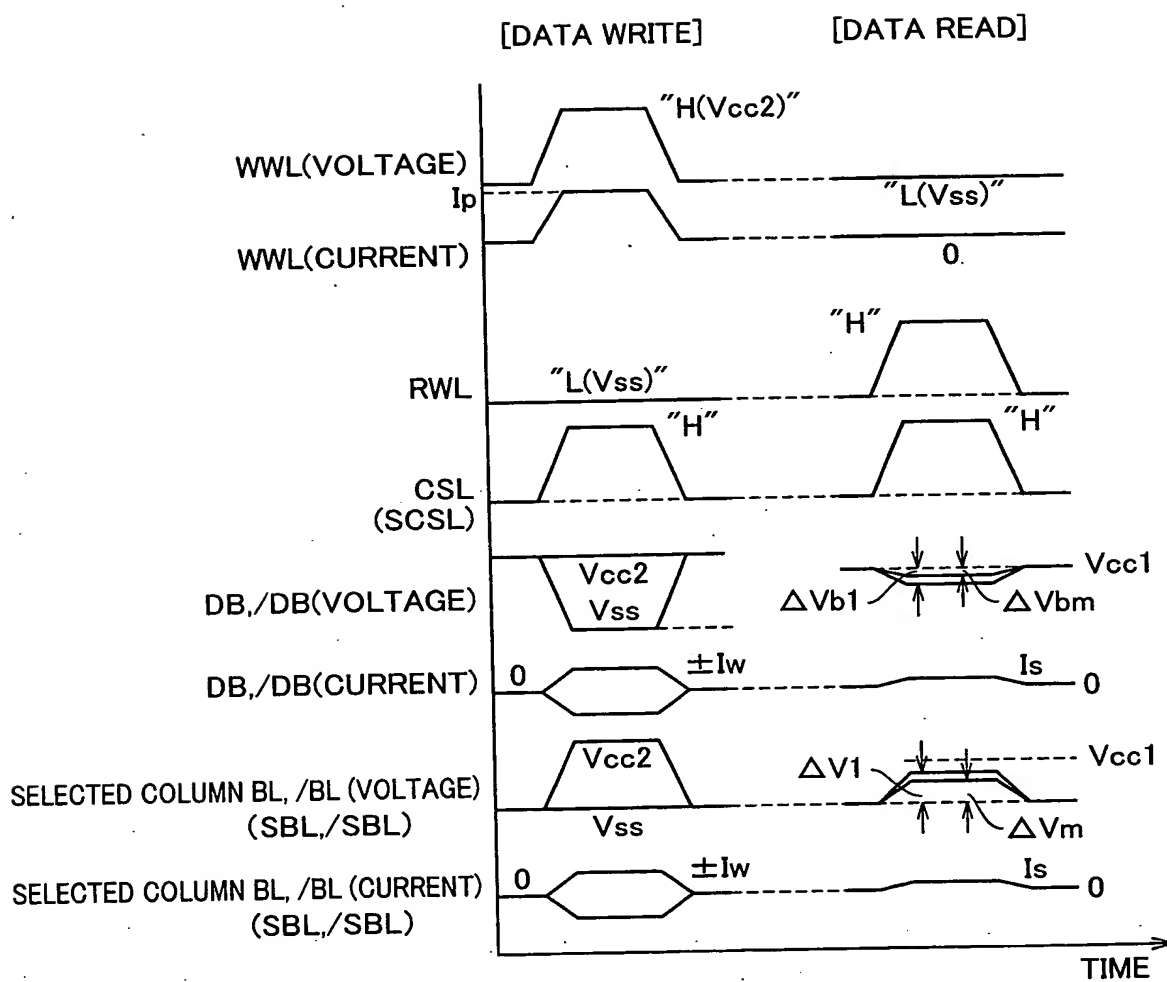


FIG. 8

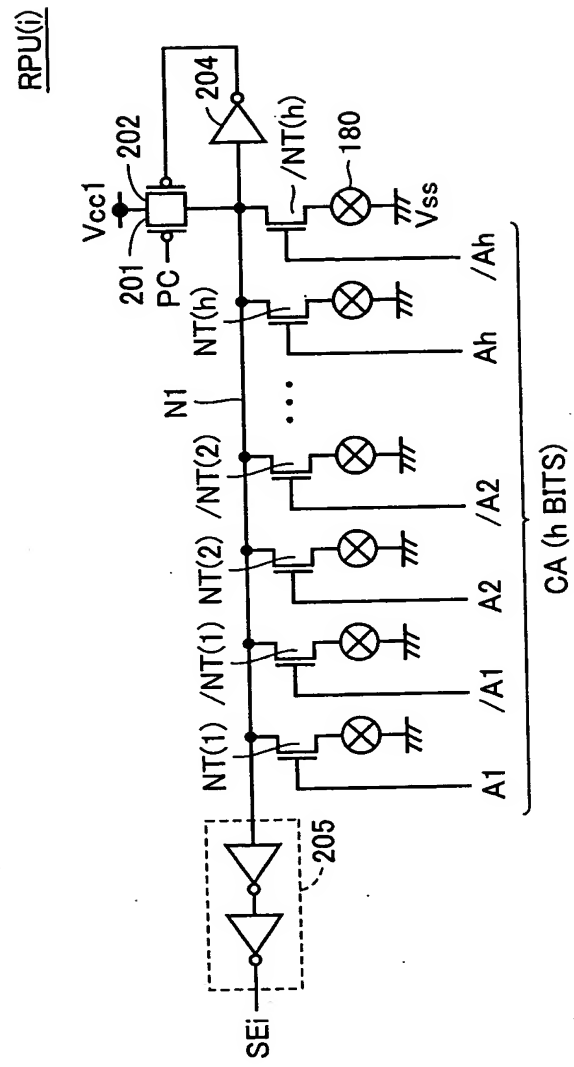


FIG.9A

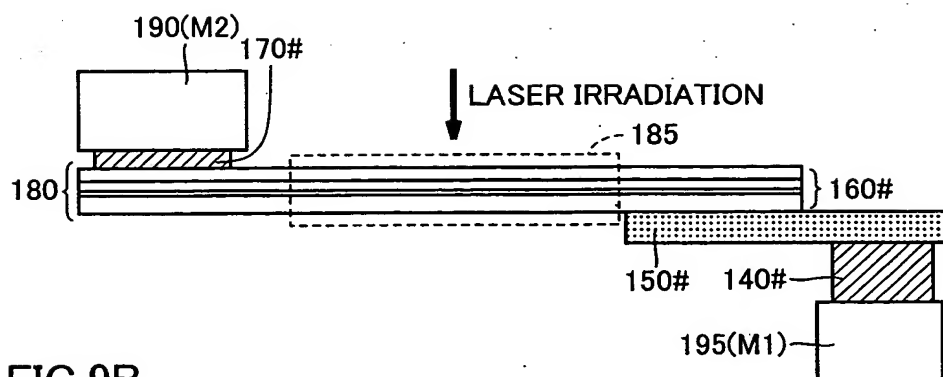


FIG.9B

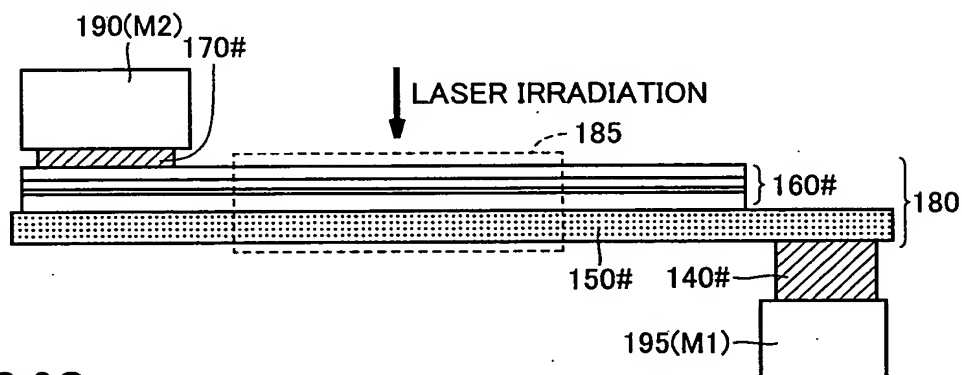


FIG.9C

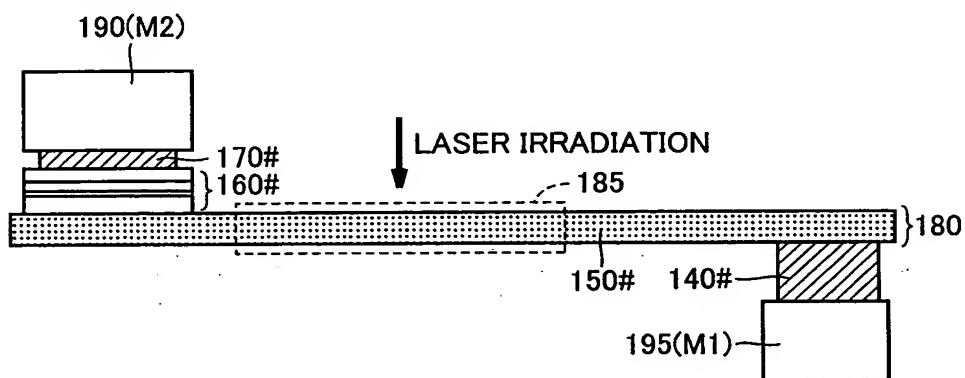


FIG.10A

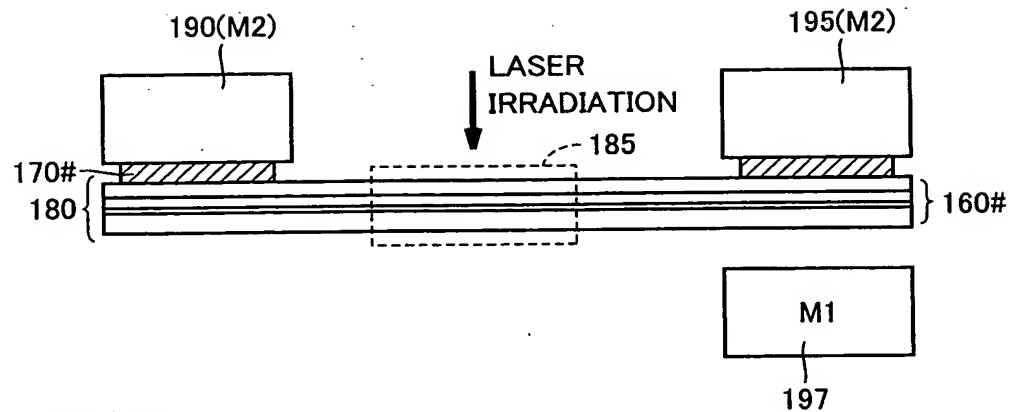


FIG.10B

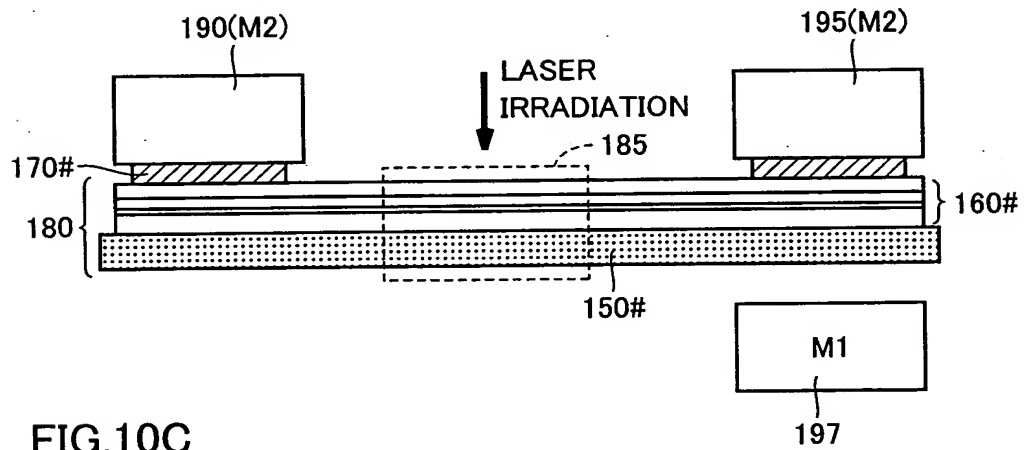


FIG.10C

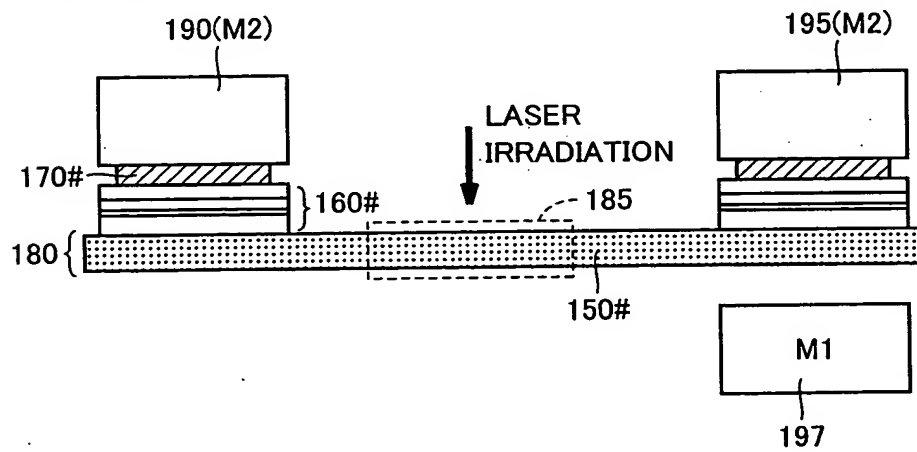


FIG.11A

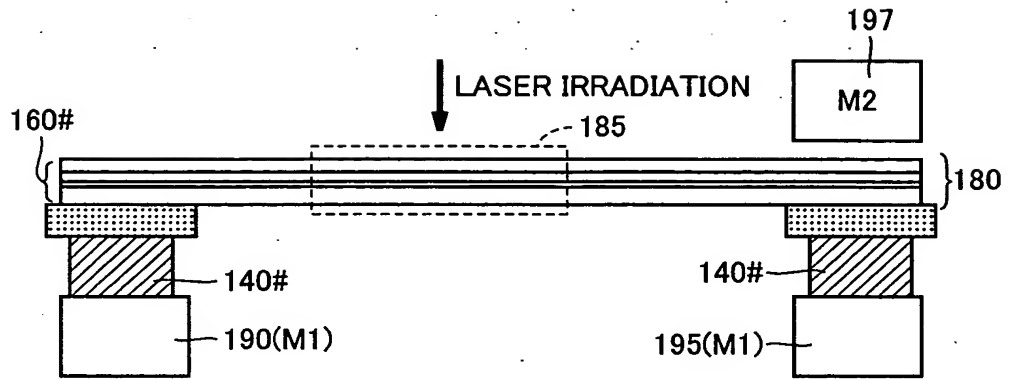


FIG.11B

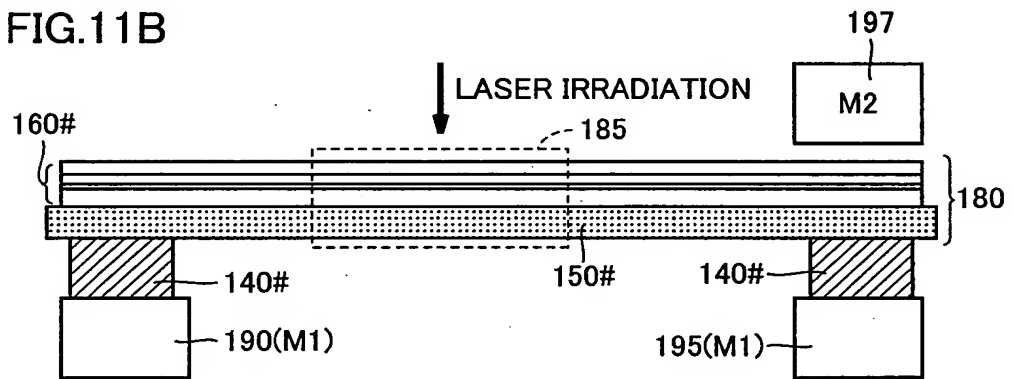


FIG.11C

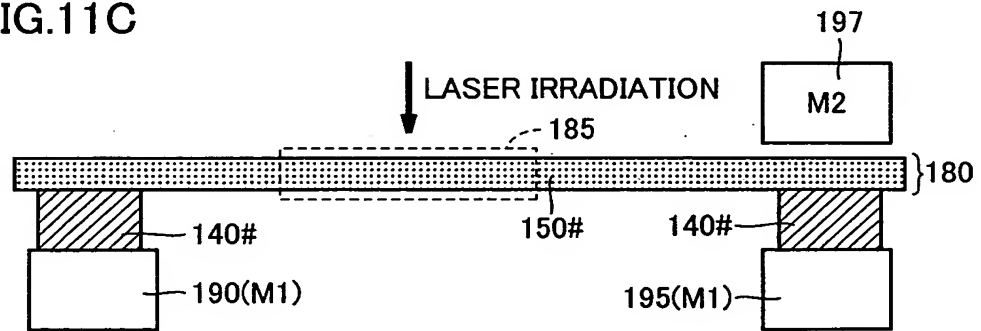


FIG.12

RPU#(i)

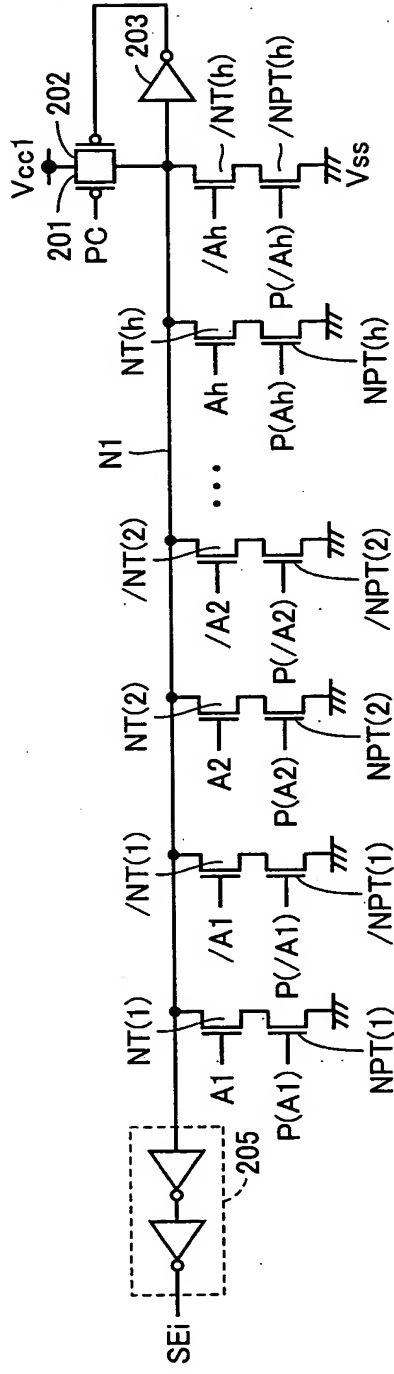


FIG.13

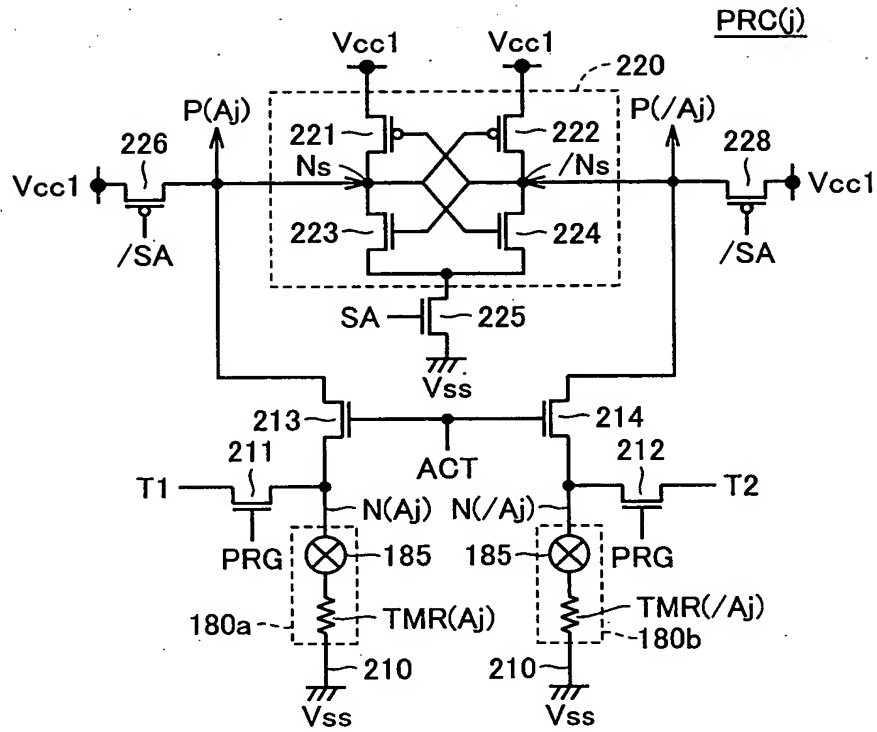


FIG.14

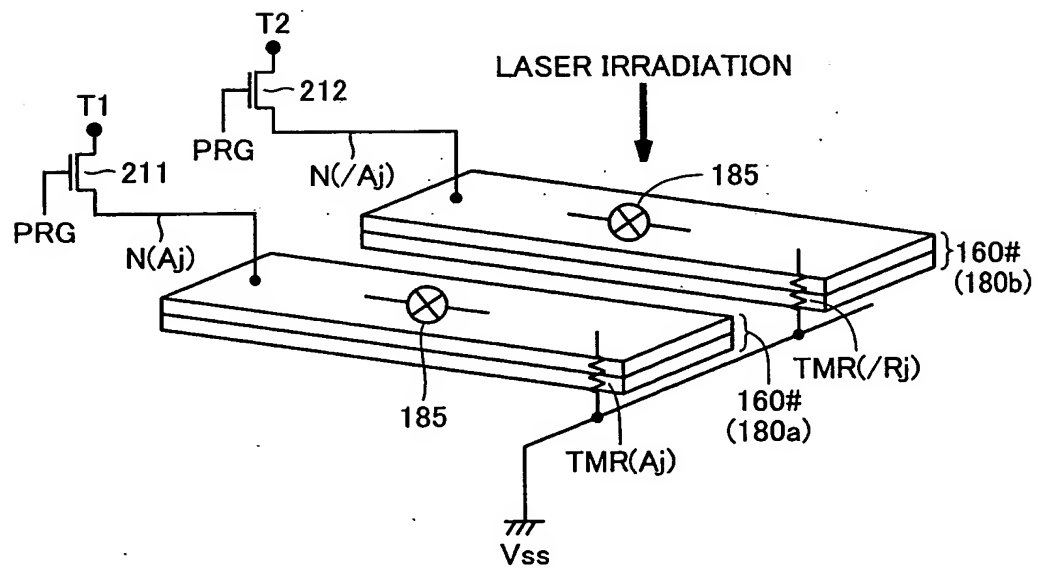


FIG.15

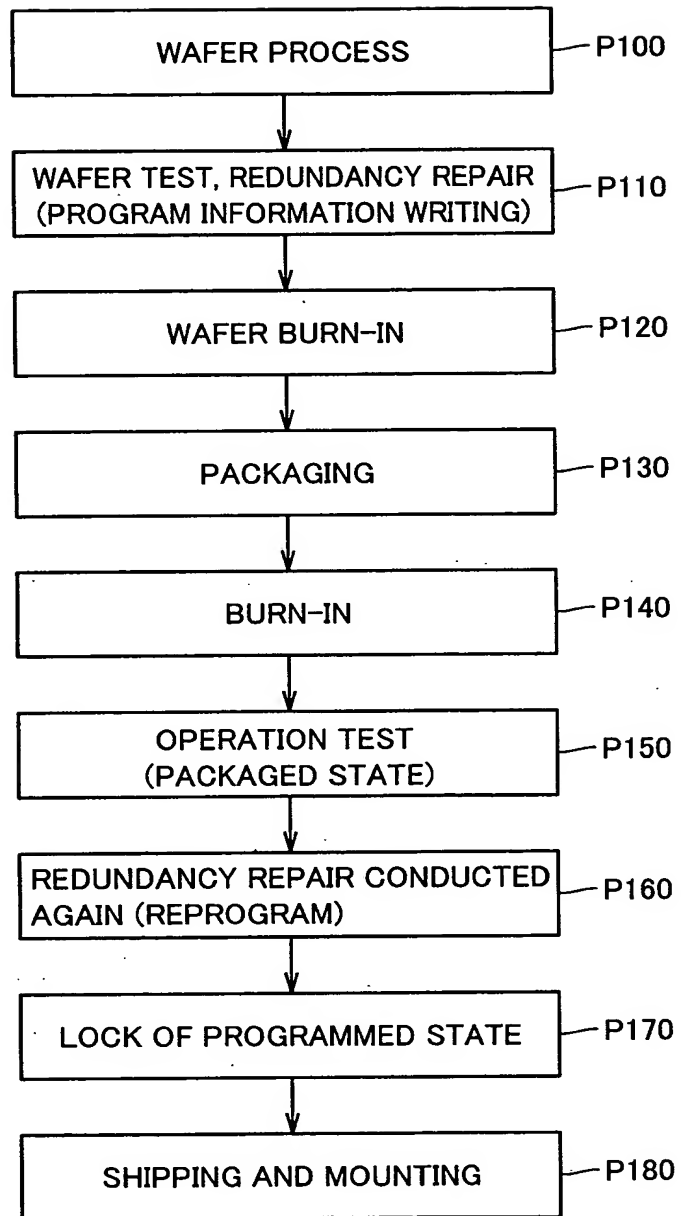


FIG.16

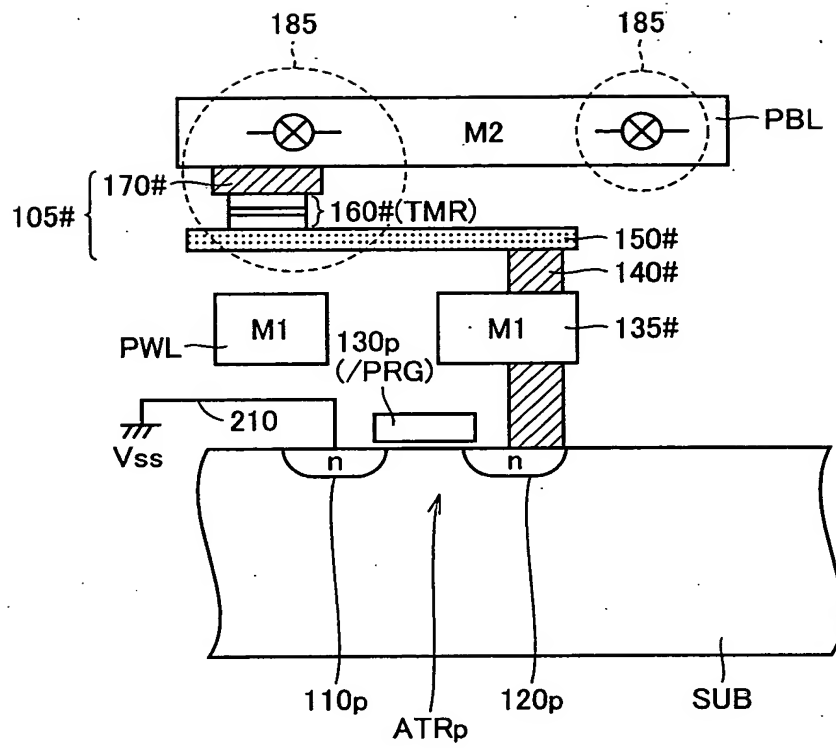
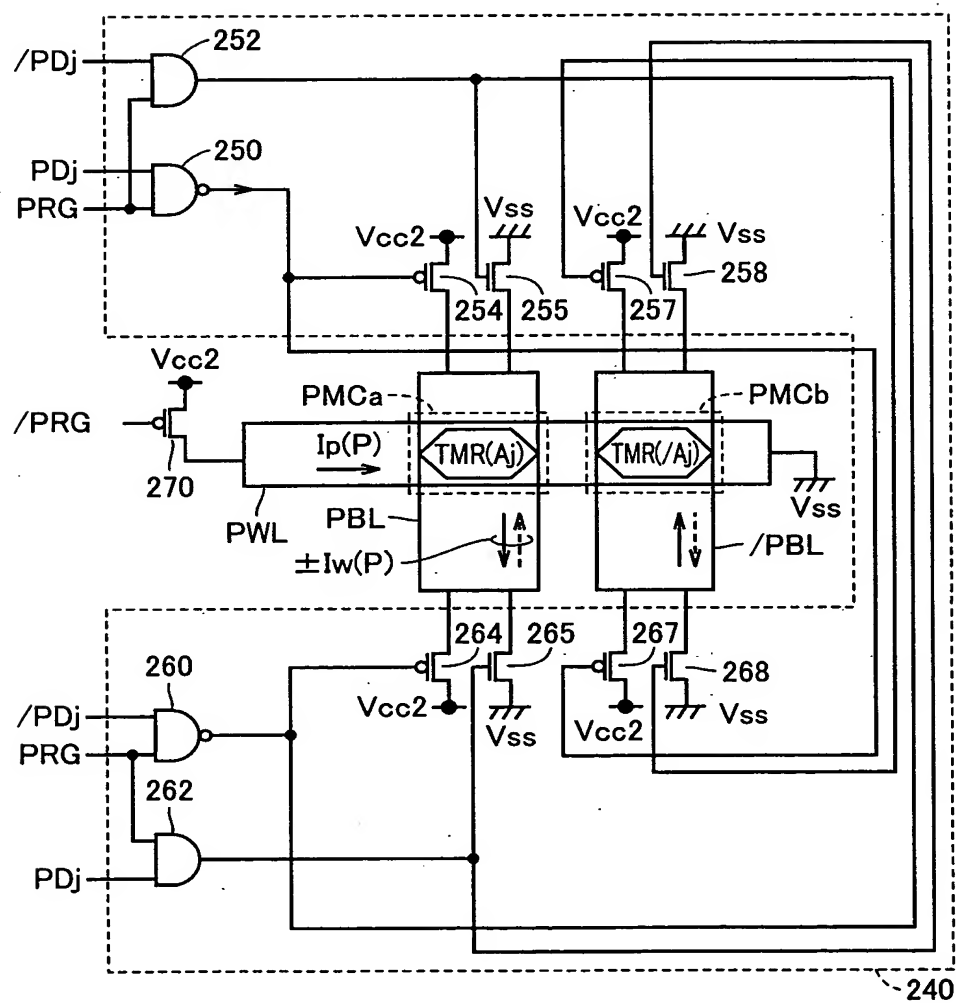


FIG. 18



The diagram illustrates a complex PLD circuit architecture. At the top, a logic core (220) is shown, which is a crossbar array of four transistors (221, 222, 223, 224) controlled by a central transistor (225). This core is connected to input buffers (226, 228) and output drivers (213, 214). The bottom section contains two programmable logic elements (PBL and /PBL), each with a programmable AND/OR array (185) and a programmable output buffer (210). The circuit is controlled by a central ACT signal and a PRG signal. Various other signals like P(Aj), P(/Aj), N(Aj), N(/Aj), TMR(Aj), TMR(/Aj), and PMCa are shown.